

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Currently Amended) A data transfer system comprising:
2 a plurality of first bus devices, at least one first bus
3 device being a first bus data supplying device capable of supplying
4 data, at least one first bus device being a first bus data
5 receiving device capable of receiving data and at least one first
6 bus device being a first bus master device capable of requesting
7 and controlling data transfer;

8 a first data bus connected to each of said plurality of first
9 bus devices and capable of transferring data from a first bus data
10 supplying device to a first bus data receiving device under control
11 of a first bus master device;

12 a plurality of second bus devices different from said
13 plurality of first bus devices, at least one second bus device
14 being a second bus data supplying device capable of supplying data,
15 at least one second bus device being a second bus data receiving
16 device capable of receiving data, a plurality of second bus devices
17 each being a second bus master device capable of requesting and
18 controlling data transfer, a predetermined one of said plurality of
19 second bus devices being a dominant second bus master device;

20 a second data bus different from said first data bus connected
21 to each of said plurality of second bus devices and capable of
22 transferring data from a second bus data supplying device to a
23 second bus data receiving device under control of a second bus
24 master device;

25 a bus bridge connected to said first data bus and said second
26 data bus, said bus bridge capable of supplying data to said first
27 bus, receiving data from said first bus, supplying data to said
28 second bus, receiving data from said second bus, not capable of

29 controlling data transfer on said first bus and capable of
30 controlling data transfer on said second bus; and
31 a second bus arbiter connected to each of said at least one
32 second bus master device, said second bus and said bus bridge, said
33 second bus arbiter granting control of data transfer on said first
34 bus to one and only one of the set of devices including each second
35 bus master and said bus bridge, said second bus arbiter granting
36 control of data transfer to said dominant second bus master
37 immediately upon request and interrupting any data transfer
38 controlled by another second bus master.

1 2. (Original) The data transfer system of claim 1, wherein:
2 said at least one first bus master device consists of a
3 central processing unit.

1 3. (Original) The data transfer system of claim 1, wherein:
2 said at least one first bus master device consists of a direct
3 memory access unit.

1 4. (Original) The data transfer system of claim 1, wherein:
2 at least one first bus supplying/receiving device consists of
3 a memory which is not capable of controlling data transfer.

1 5. (Currently Amended) The data transfer system of claim 1,
2 wherein:
3 each second bus master generates a corresponding bus request
4 signal to said second bus arbiter for second bus to request control
5 of said second bus, said second bus arbiter having grant logic
6 corresponding to each second bus master supplying a bus grant
7 signal to said corresponding bus master upon bus grant, said bus
8 request signal of said dominant bus master supplied to said grant

9 logic corresponding to every other second bus masters for
10 inhibiting generation of said grant request.

1 6. (Original) The data transfer system of claim 5, wherein:
2 said bus arbiter grants control of said second bus to second
3 bus master devices other than dominant bus master in a round robin
4 fashion.

1 7. (Currently Amended) The A data transfer system ~~of claim 1,~~
2 wherein comprising:

3 a plurality of first bus devices, at least one first bus
4 device being a first bus data supplying device capable of supplying
5 data, at least one first bus device being a first bus data
6 receiving device capable of receiving data, and at least one first
7 bus device being a first bus master device capable of requesting
8 and controlling data transfer and at least one first bus
9 supplying/receiving device consists of being a central processing
10 unit which is further capable of controlling data transfer; and

11 a first data bus connected to each of said plurality of first
12 bus devices and capable of transferring data from a first bus data
13 supplying device to a first bus data receiving device under control
14 of a first bus master device;

15 a plurality of second bus devices, at least one second bus
16 device being a second bus data supplying device capable of
17 supplying data, at least one second bus device being a second bus
18 data receiving device capable of receiving data, a plurality of
19 second bus devices each being a second bus master device capable of
20 requesting and controlling data transfer, a predetermined one of
21 said plurality of second bus devices being a dominant second bus
22 master device said at least one second bus master device is
23 responsive to real time events asynchronous to operation of said
24 central processing unit;

25 a second data bus connected to each of said plurality of
26 second bus devices and capable of transferring data from a second
27 bus data supplying device to a second bus data receiving device
28 under control of a second bus master device;

29 a bus bridge connected to said first data bus and said second
30 data bus, said bus bridge capable of supplying data to said first
31 bus, receiving data from said first bus, supplying data to said
32 second bus, receiving data from said second bus, not capable of
33 controlling data transfer on said first bus and capable of
34 controlling data transfer on said second bus; and

35 a second bus arbiter connected to each of said at least one
36 second bus master device, said second bus and said bus bridge, said
37 second bus arbiter granting control of data transfer on said first
38 bus to one and only one of the set of devices including each second
39 bus master and said bus bridge, said second bus arbiter granting
40 control of data transfer to said dominant second bus master
41 immediately upon request and interrupting any data transfer
42 controlled by another second bus master.

1 8. (New) The data transfer system of claim 7, wherein:
2 said at least one first bus master device consists of a direct
3 memory access unit.

1 9. (New) The data transfer system of claim 7, wherein:
2 at least one first bus supplying/receiving device consists of
3 a memory which is not capable of controlling data transfer.

1 10. (New) The data transfer system of claim 7, wherein:
2 each second bus master generates a corresponding bus request
3 signal to said second bus arbiter for second bus to request control
4 of said second bus, said second bus arbiter having grant logic
5 corresponding to each second bus master supplying a bus grant

6 signal to said corresponding bus master upon bus grant, said bus
7 request signal of said dominant bus master supplied to said grant
8 logic corresponding to every other second bus masters for
9 inhibiting generation of said grant request.

1 11. (New) The data transfer system of claim 10, wherein:
2 said bus arbiter grants control of said second bus to second
3 bus master devices other than dominant bus master in a round robin
4 fashion.